

Nonlinear Circuit Design Using the Modified Harmonic Balance Algorithm

R. Gilmore. "Nonlinear Circuit Design Using the Modified Harmonic Balance Algorithm." 1986 Transactions on Microwave Theory and Techniques 34.12 (Dec. 1986 [T-MTT] (1986 Symposium Issue)): 1294-1307.

A modification to a harmonic balance algorithm allows the nonlinear analysis of circuits driven by two nonharmonically related input frequencies. The algorithm was implemented on an IBM AT Personal Computer. Three examples are presented to illustrate the analysis. The first is a novel wide-band FET frequency doubler that achieves an average conversion loss of 3.5 dB over the 8-16-GHz output band. The second example illustrates a technique used in the design of a C-band power amplifier in which third-order intermodulation distortion was reduced by 8 dB with two tones of 34 dBm each at the output. The final example illustrates the gain suppression of a smaller tone in the presence of a larger one of slightly different frequency in a limiting amplifier. Simulations agree with measurements in which 2.5-dB gain suppression was observed in a 2-GHz FET feedback amplifier driven into saturation.

 [Return to main document.](#)